REMARKS

This Amendment responds to the Office Action mailed March 26, 2004 in the above-identified application. Based on the foregoing amendments and the following comments, reconsideration and allowance of the application are respectfully requested.

Claims 1-14 were pending in this application. By this Amendment, claims 1-6 and 12-14 have been canceled without prejudice or disclaimer. New claim 15 has been added. Accordingly, claims 7-11 and 15 are pending in the application. Claim 7 is an independent claim. No new matter has been added.

Applicants mailed an Appeal Brief in this application on December 22, 2003. In response, the Examiner has reopened prosecution and has set forth new grounds for rejection. The rejection is respectfully traversed.

The Examiner has rejected claims 1-6 and 12-14 under 35 U.S.C. §102(e) as anticipated by Nakamatsu et al. (U.S. 6,473,822). Claims 7-11 are rejected under 35 U.S.C. §103(a) as unpatentable over Tobita et al. (U.S. 5,530,673) in view of Nakamatsu.

Nakamatsu discloses digital signal processing apparatus including a main CPU and an extension processor. As shown in Fig. 9 of Nakamatsu, expansion board 54 is provided with board ID circuit 67, which may be a ROM (col. 9, lines 9-28).

Tobita discloses a flash memory control method and system. Fig. 87 of Tobita shows a main memory system using a flash memory. Fig. 97 is a schematic diagram of a flash memory. Fig. 86 illustrates a single flash memory chip.

Claim 7 is directed to a computer storage system comprising an array of storage devices, a system cache memory, and a plurality of controller boards for controlling data transfer to and between the array of storage devices, the system cache memory and a host computer. Each of the controller boards has electronic circuitry including a non-volatile memory containing product data that identifies the respective controller board and means for reading the product data in the non-volatile memory.

An example of a computer storage system as defined by claim 7 is shown in Fig. 1 of the present application. The storage system includes one or more front end directors 20, 22, ... 24, which are responsible for translating read/write requests from a host computer 10 into requests to disk drives 50, 52, etc. The front end directors are connected to a system cache memory 40, and

the system cache memory is coupled to the disk drives 50, 52, etc. through back end directors 60, 62, ... 64. The system may be implemented as a plurality of printed circuit boards mounted in a backplane. Each director may be packaged as a printed circuit board. The backplane provides interconnections between the directors, the system cache memory, the host computer and the disk drives. Each director board may include a non-volatile memory which stores product data that uniquely identifies the director board.

The Examiner asserts that Tobita discloses a computer storage system comprising an array of storage devices, a system cache memory and a plurality of controller boards, with reference to Figs. 87 and 97 of Tobita. The assertion that Tobita discloses a plurality of controller boards is respectfully traversed. Fig. 97 of Tobita illustrates the architecture of a flash memory (col. 17, lines 50-51 and col. 1, lines 38-59). The flash memory is shown in Fig. 97 to include a control circuit 4105. Fig. 86 of Tobita and the accompanying description at col. 50, lines 23-30 state that numeral 4031 represents a flash memory chip. The memory system shown in Fig. 87 thus includes a plurality of flash memory chips. Accordingly, it is submitted that Tobita does not disclose or even remotely suggest a plurality of controller boards for controlling data transfer to and between an array of storage devices, a system cache memory and a host computer, as required by Applicants' claim 7. The control circuits shown in Fig. 97 of Tobita are circuits on each flash memory chip rather than controller boards. Furthermore, the control circuits of Tobita are part of the flash memory chips rather than separate controller boards which control data transfer to and between the array of storage devices, the system cache memory and the host computer. In summary, Tobita discloses a plurality of *flash memory chips*, each including *a control circuit within the chip*, but does not disclose a plurality of *controller boards* as claimed. Accordingly, Tobita does not disclose or suggest a computer storage system as claimed.

Because Tobita does not disclose controller boards, the combination of Tobita and Nakamatsu is improper. It is well established that one of the three basic criteria for a *prima facie* case of obviousness is that there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings (MPEP §2143). It is submitted that the Examiner has failed to establish a suggestion or motivation to combine the reference teachings.

No reason is apparent why one of skill in the art would utilize the board ID circuit disclosed by Nakamatsu in the flash memory system disclosed by Tobita or why one of skill in the art would consult Nakamatsu at all in connection with the flash memory system disclosed by Tobita. Tobita does not disclose controller boards and thus has no need for a board ID circuit. Accordingly, the combination of Tobita and Nakamatsu is improper and does not establish a *prima facie* case of obviousness.

For these reasons, claim 7 is clearly and patentably distinguished over Tobita in view of Nakamatsu. Claims 8-11 and new claim 15 depend from claim 7 and are patentable over Tobita in view of Nakamatsu for at least the reasons discussed above in connection with claim 7. New claim 15 specifies that the storage devices comprise disk drives. The cited references do not disclose or suggest storage devices comprising disk drives. Accordingly, claims 7-11 and 15 are patentable over Tobita in view of Nakamatsu.

CONCLUSION

In view of the foregoing amendments and remarks, this application should now be in condition for allowance. A notice to this effect is respectfully requested. If the Examiner believes, after this amendment, that the application is not in condition for allowance, the Examiner is requested to call the Applicant's attorney at the telephone number listed below.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

Respectfully submitted,
Scaringella et al., Applicants

By: William R. McClellan

William R. McClellan, Reg. No. 29,409
Wolf, Greenfield & Sacks, P.C.
600 Atlantic Avenue
Boston, Massachusetts 02210-2211
Telephone: (617) 720-3500

Docket No. E0295.70126US00
Date: June 14, 2004
x06/26/04x